

FIG. 1

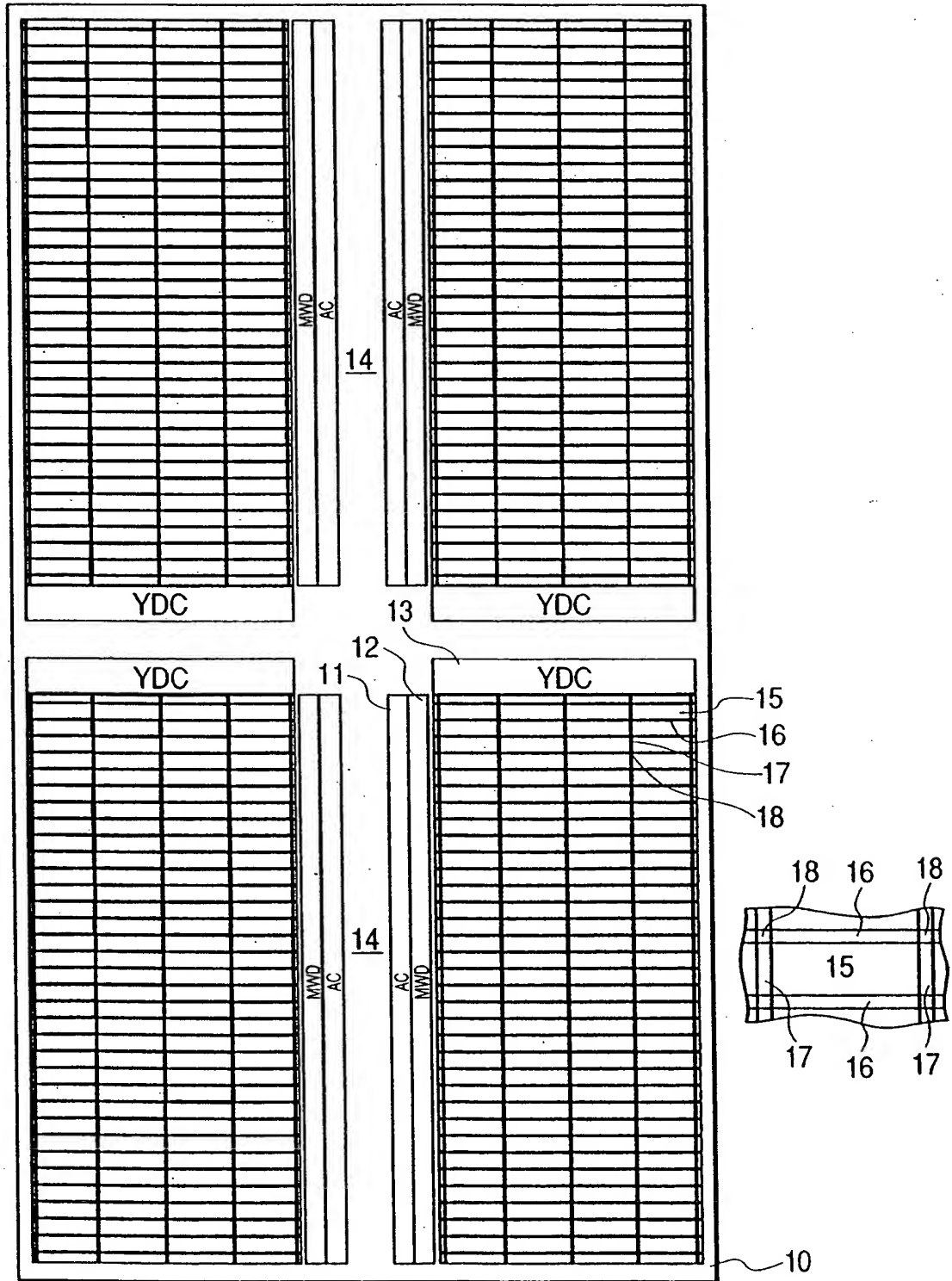


FIG. 2A

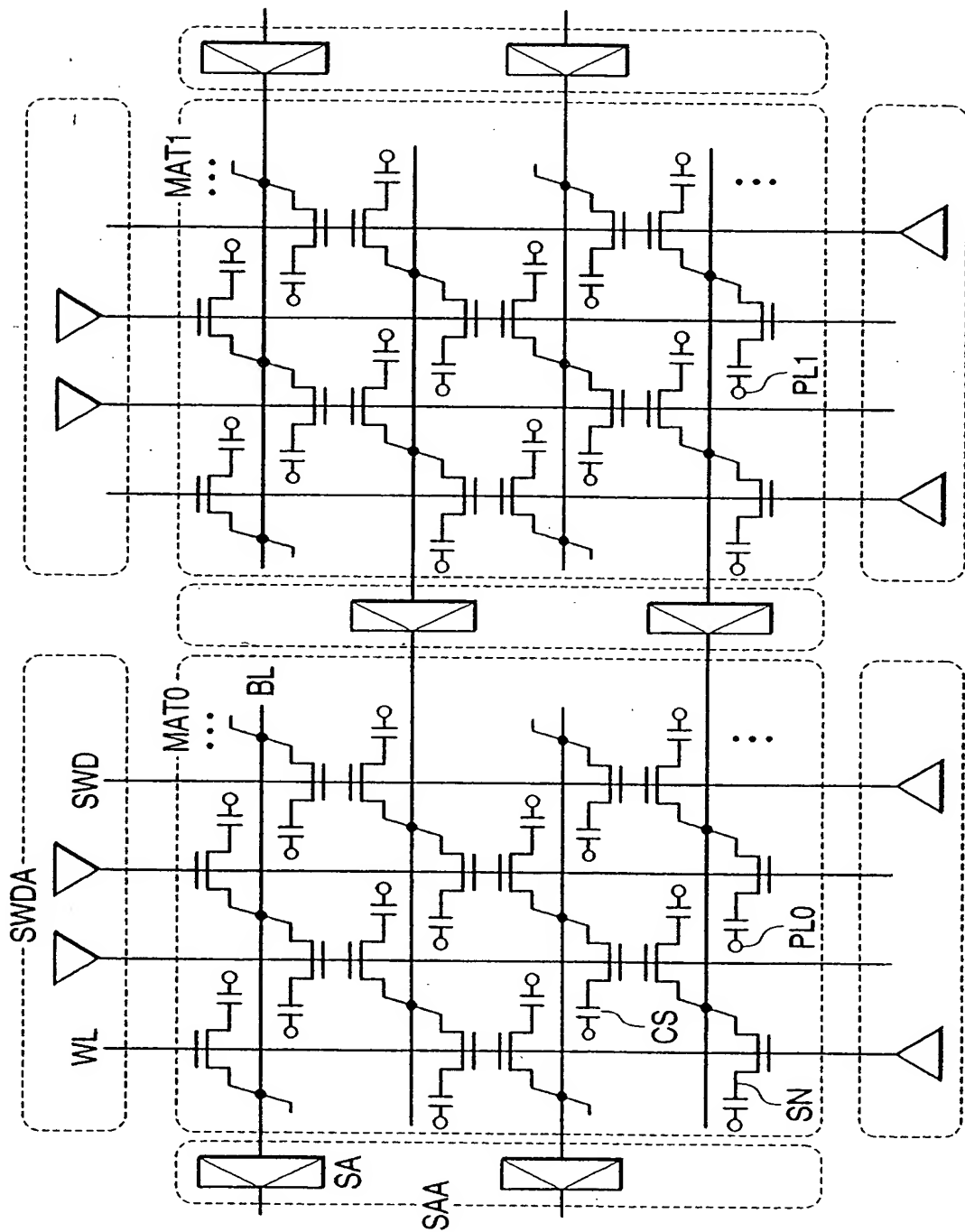


FIG. 2B

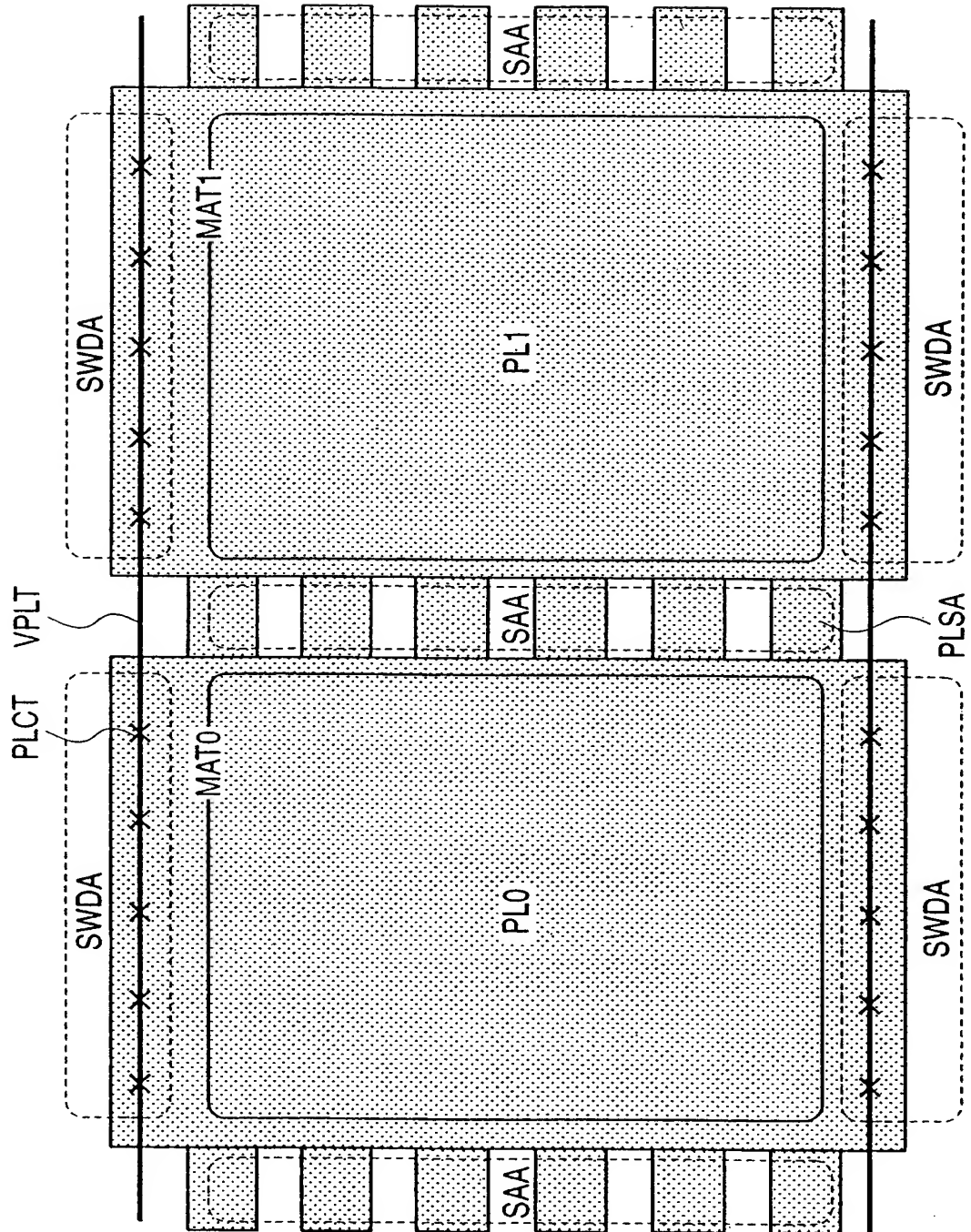


FIG. 3A

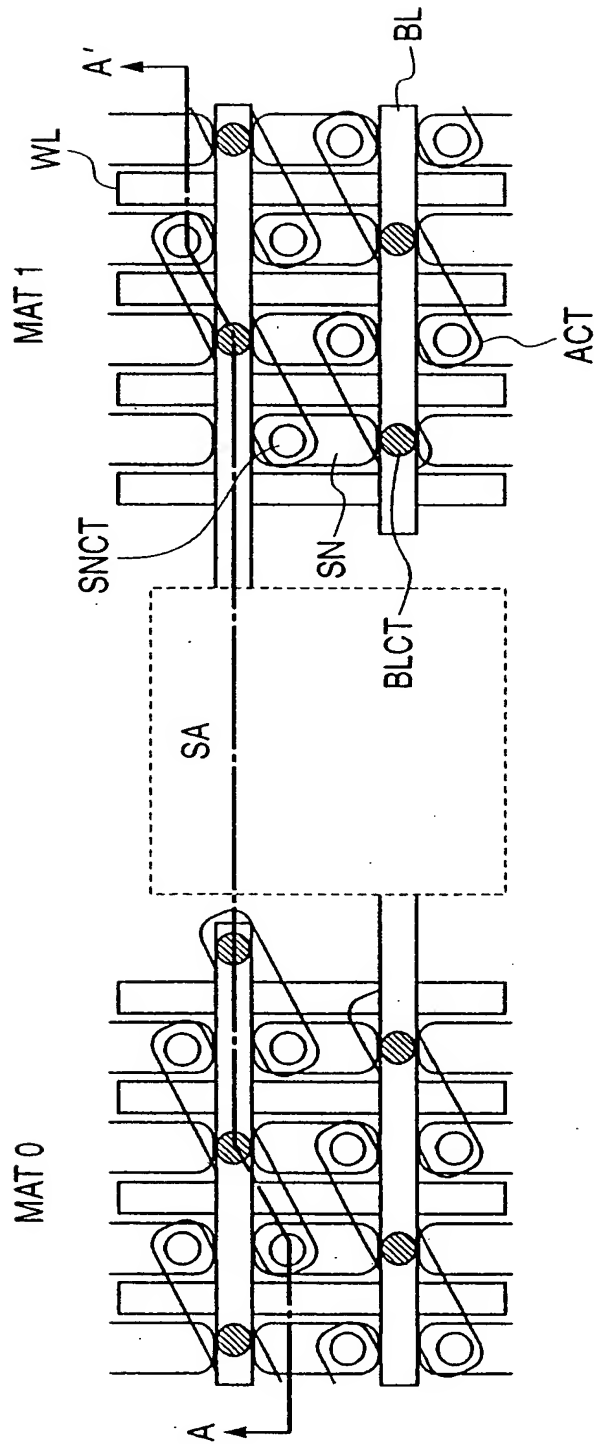


FIG. 3B

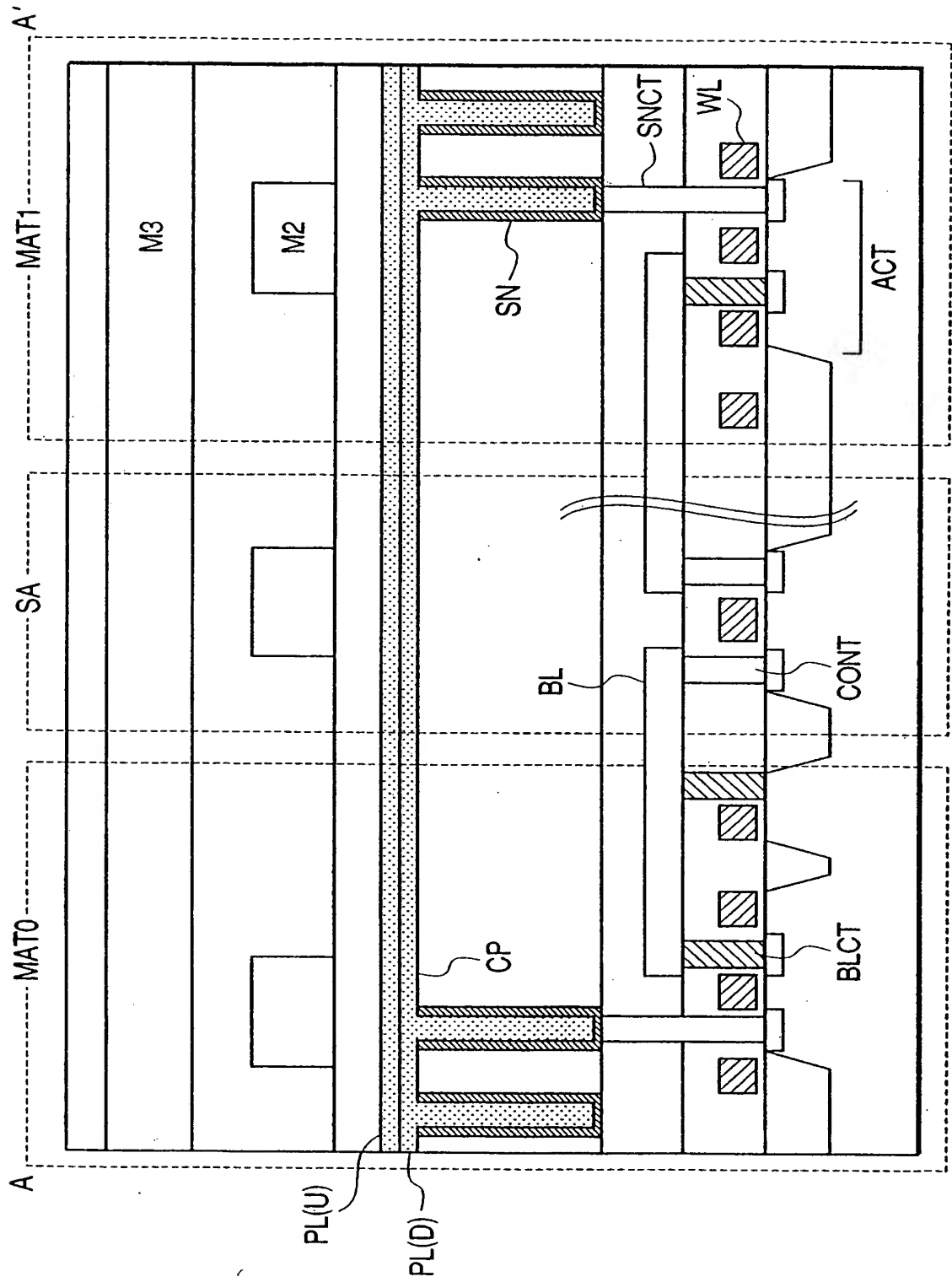
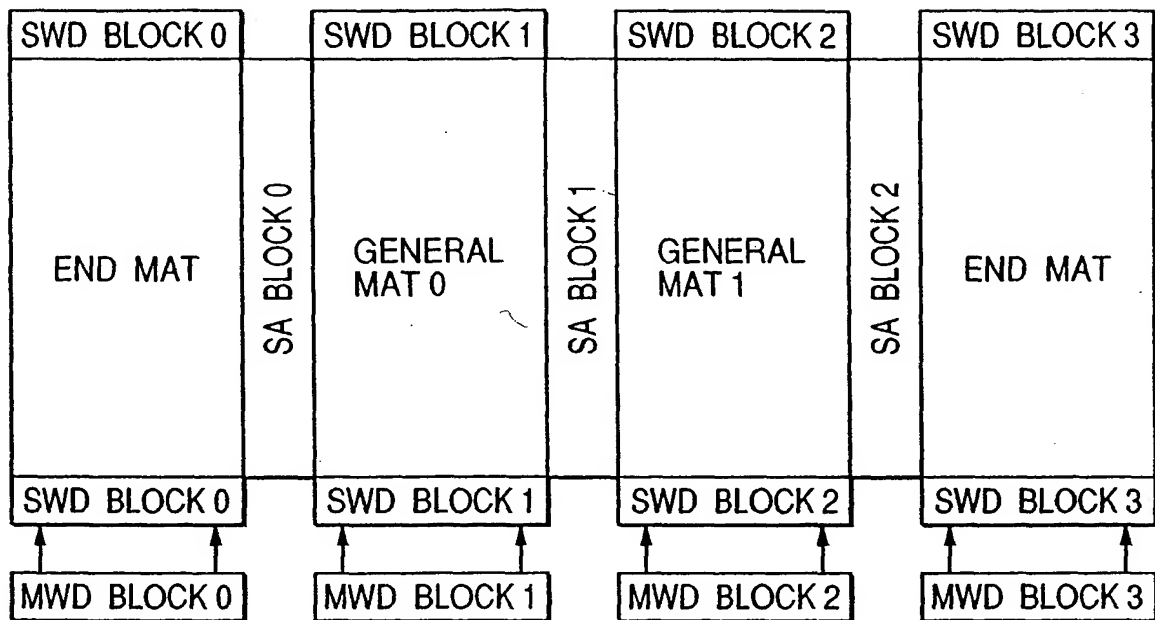
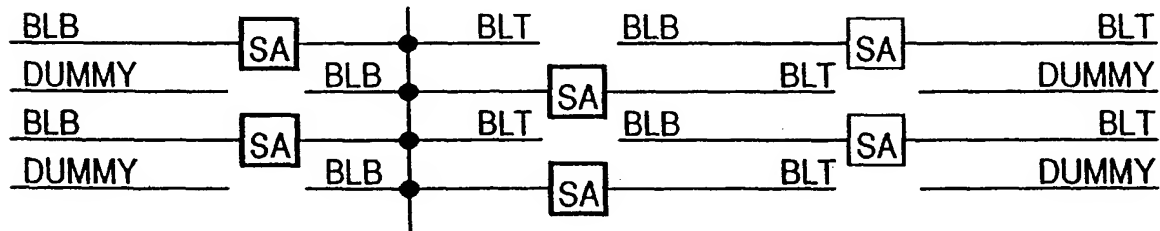


FIG. 4A**FIG. 4B**

IN ACCESSING GENERAL MAT 0:
 SWD BLOCK 1: ACTIVATED
 SA BLOCKS 0,1: ACTIVATED

**FIG. 4C**

IN ACCESSING END MAT:
 SWD BLOCKS 0,3: CONCURRENTLY ACTIVATED
 SA BLOCKS 0,2: ACTIVATED

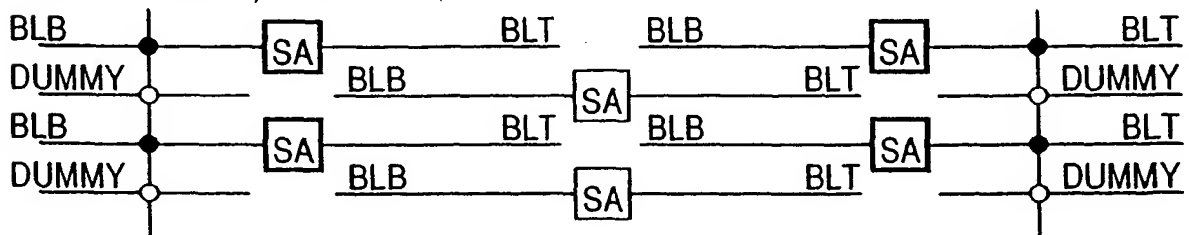
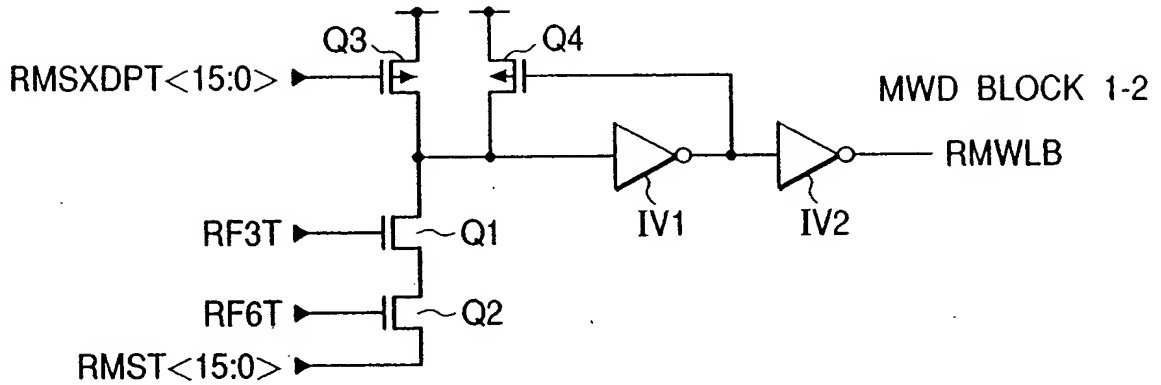
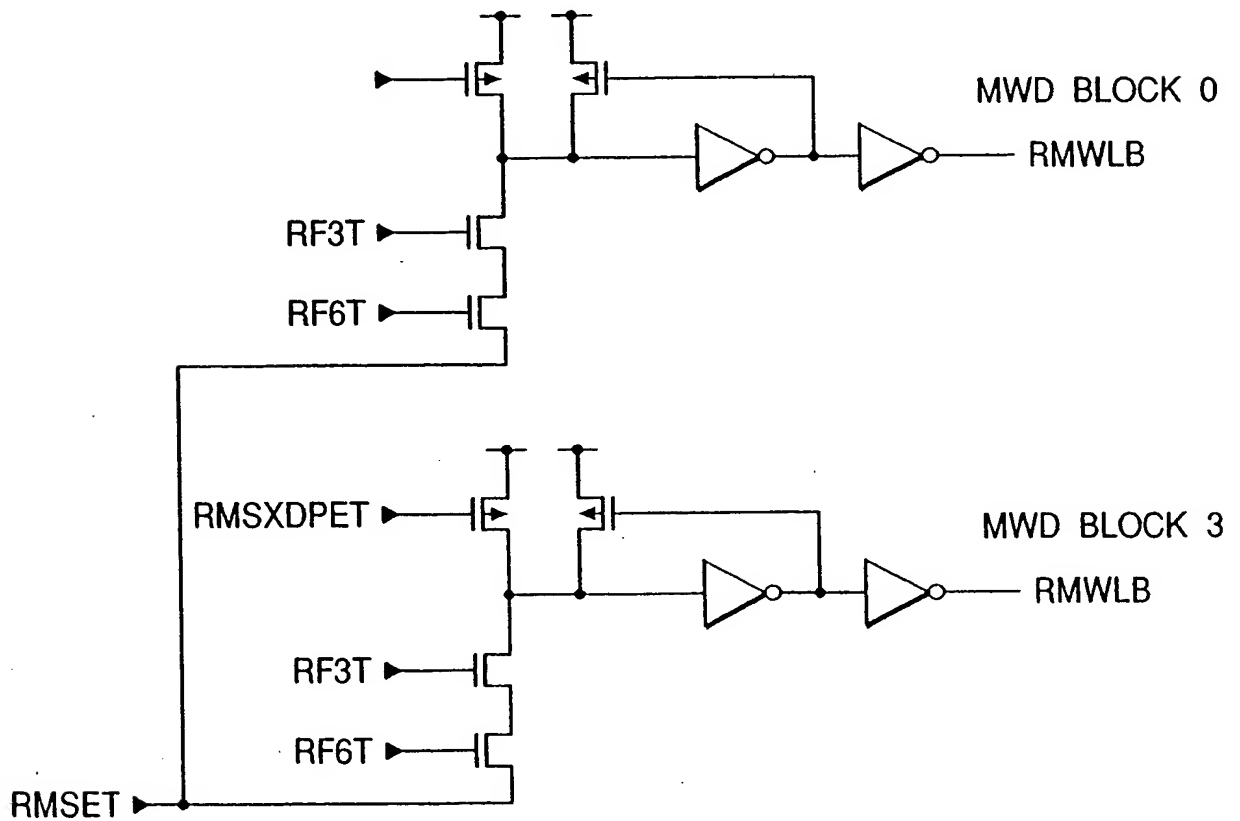


FIG. 5A

GENERAL MAT MWD CIRCUIT EXAMPLE

**FIG. 5B**

END MAT MWD CIRCUIT EXAMPLE



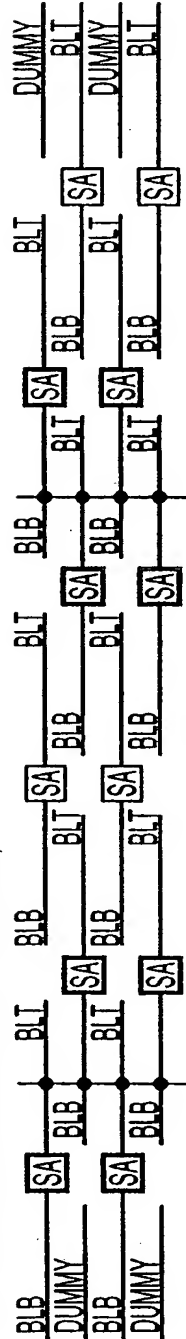
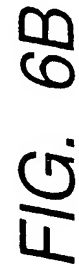
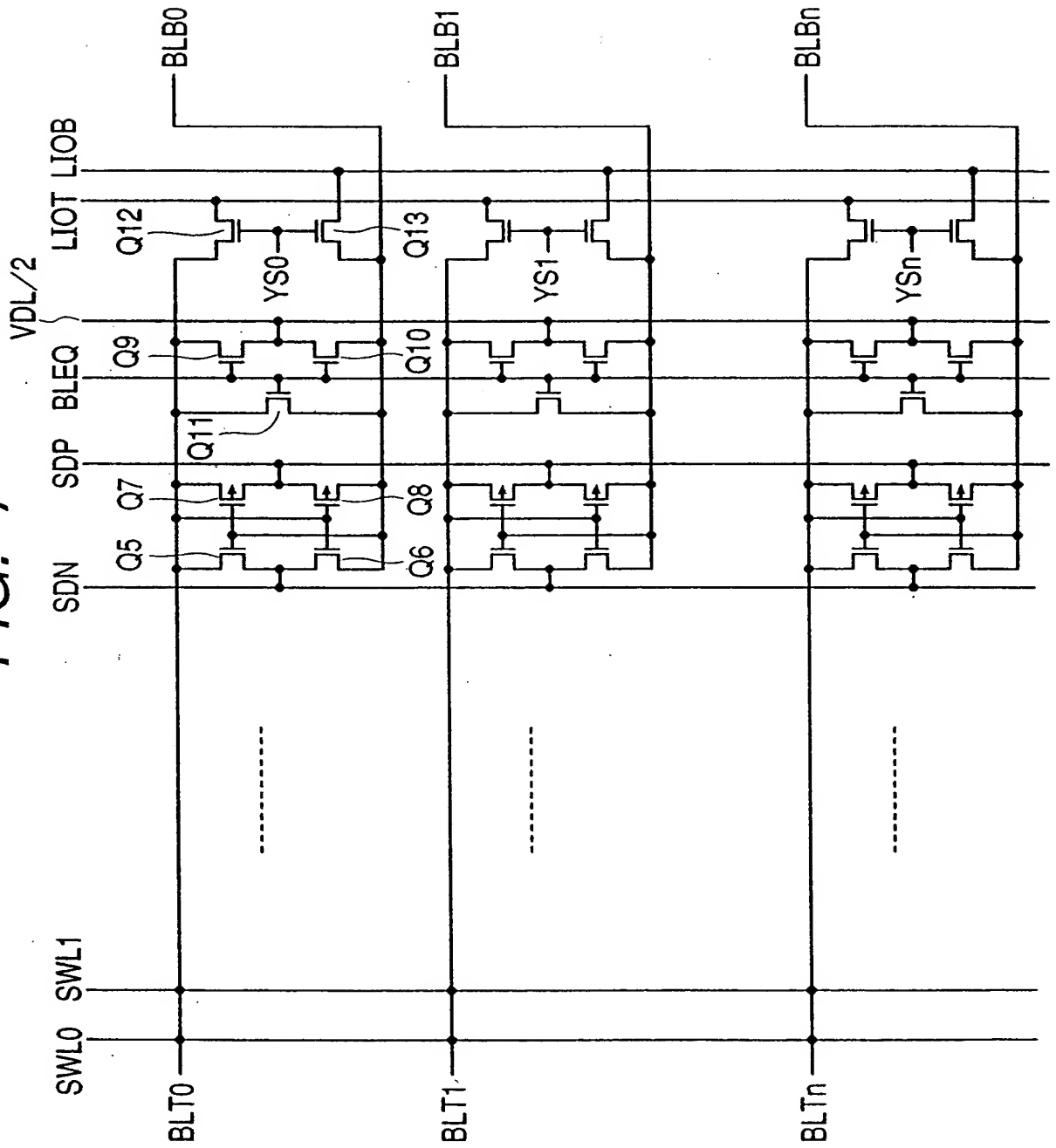


FIG. 6C

FIG. 7



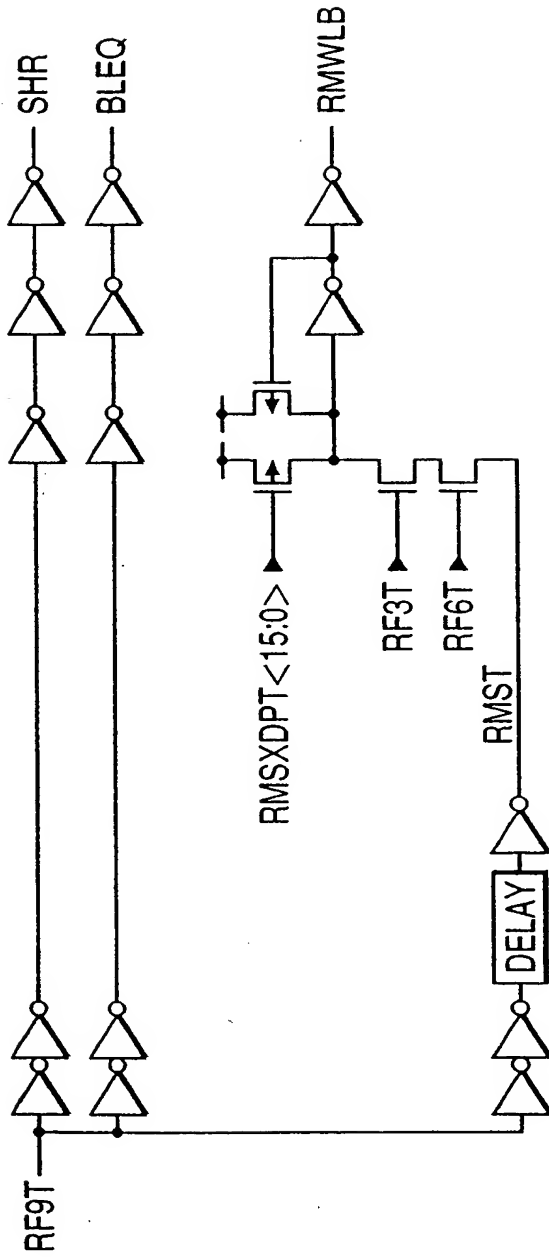


FIG. 8A

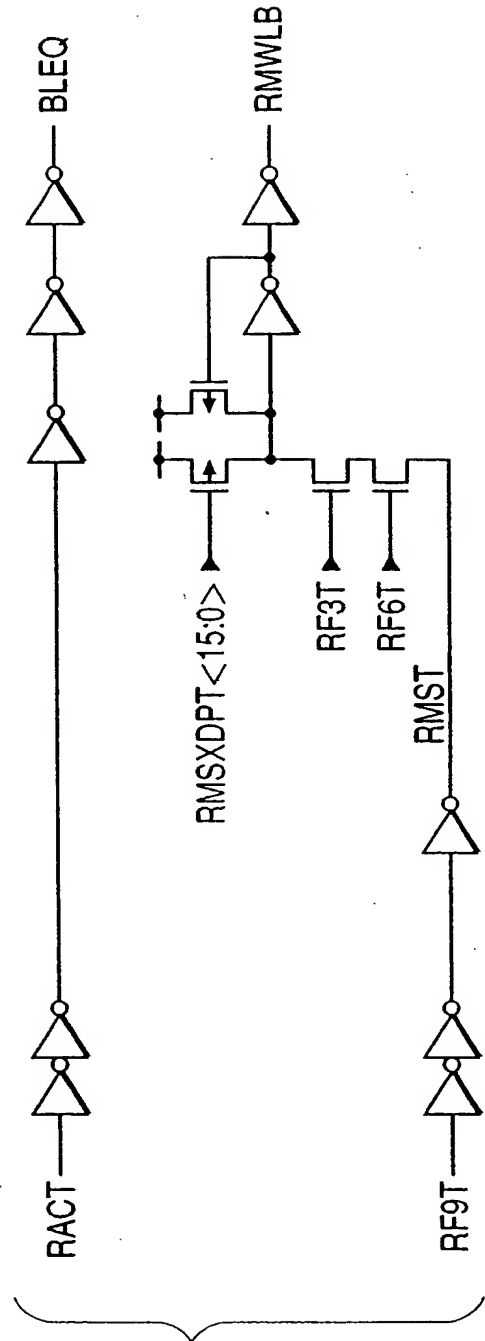
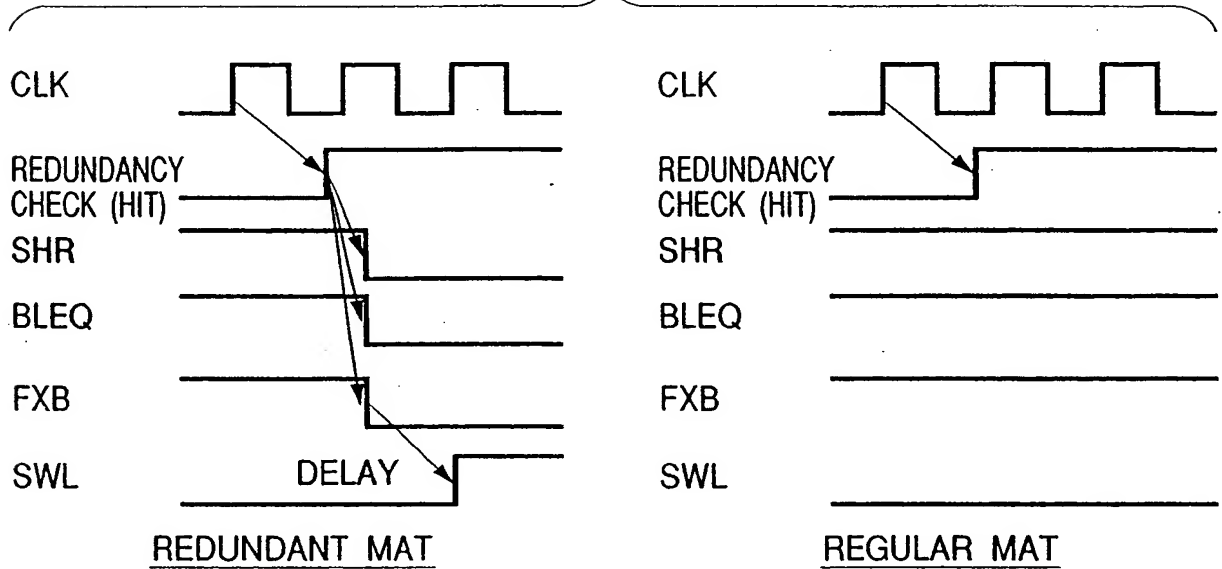


FIG. 8B

FIG. 9A

DELAYS FOR ALLOCATING BLEQ/
SHR \leftrightarrow SWL TIMING MARGIN ARE REQUIRED :

**FIG. 9B**

NO DELAYS FOR ALLOCATING BLEQ \leftrightarrow SWL TIMING
MARGIN ARE REQUIRED :

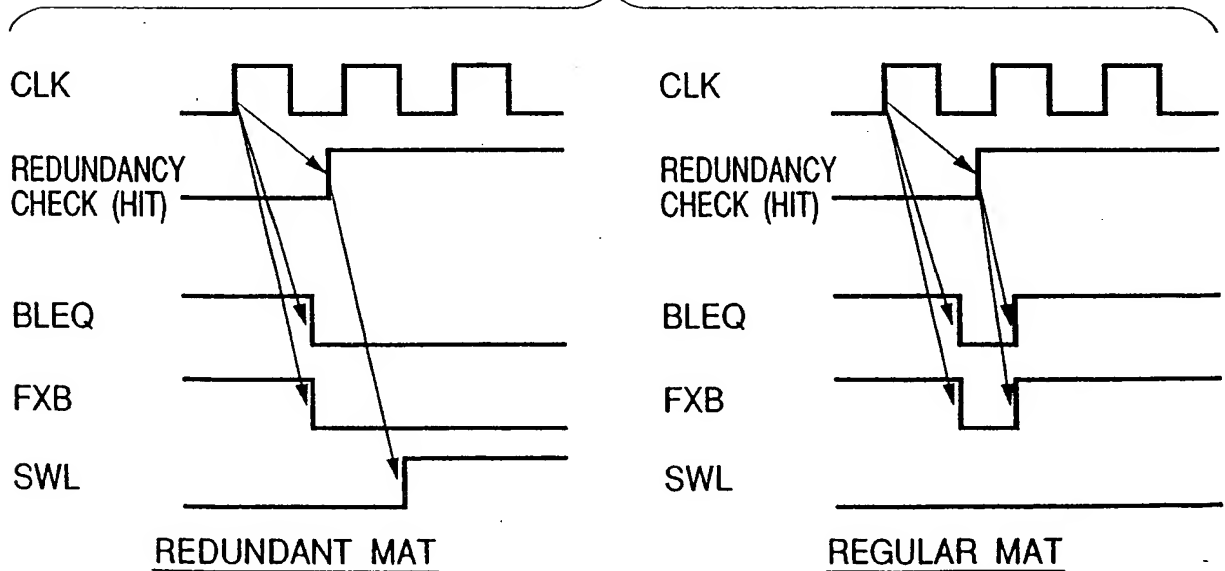


FIG. 10

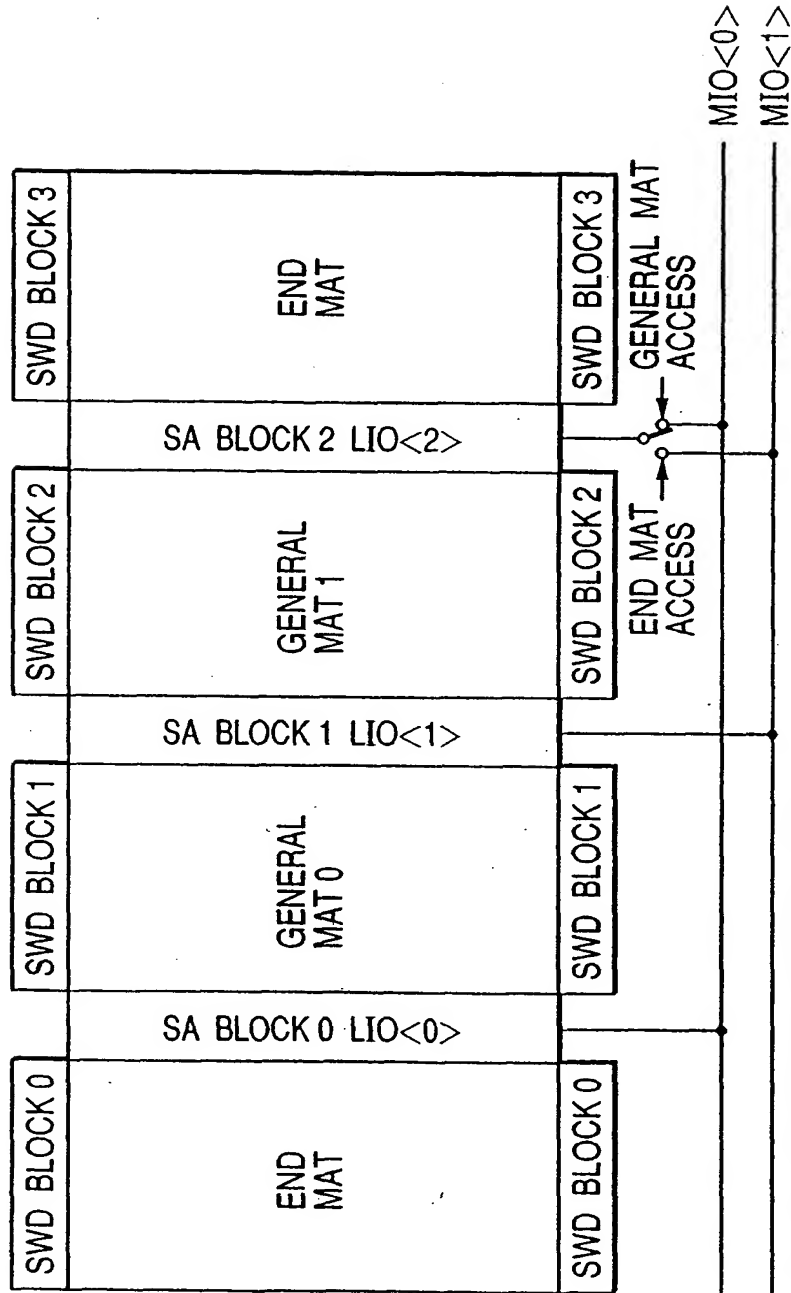


FIG. 11A
GENERAL MATS ON BOTH SIDES

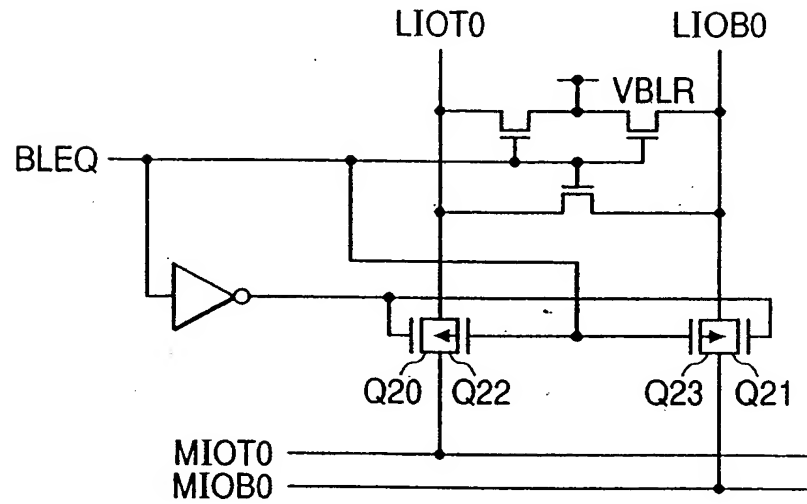


FIG. 11B
END MAT ON ONE SIDE

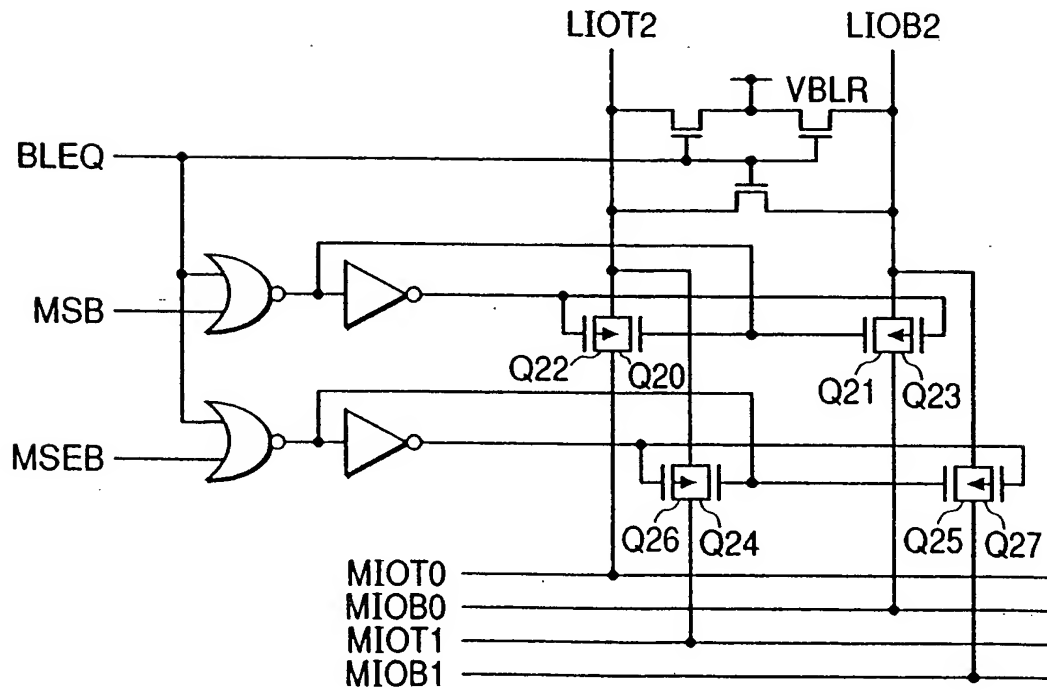
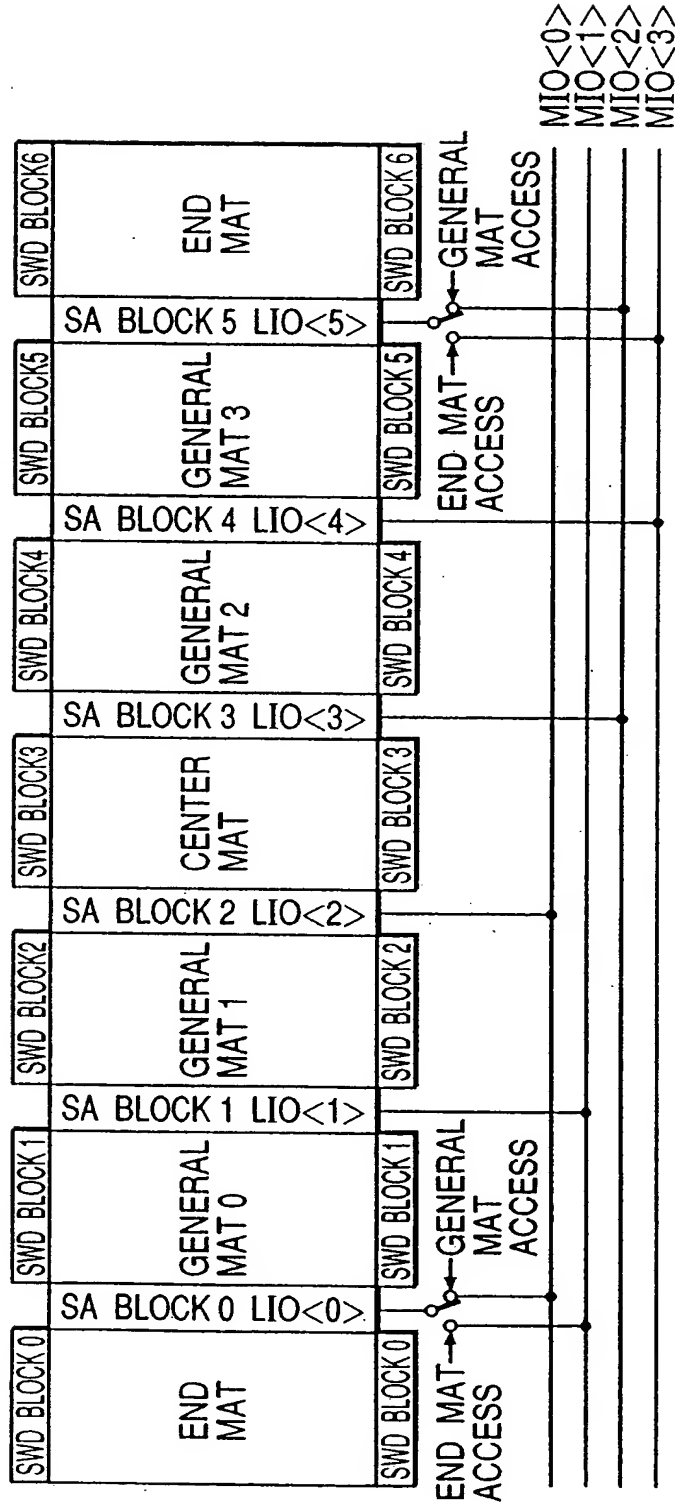


FIG. 12



(a) IN ACCESSING GENERAL MATS 0,2:

CONNECT LIO<0> AND MIO<0>, LIO<1> AND MIO<1>, LIO<3> AND MIO<2>, AND LIO<4> AND MIO<3>, RESPECTIVELY

(b) IN ACCESSING END AND CENTER MATS:

CONNECT LIO<0> AND MIO<1>, LIO<2> AND MIO<0>, LIO<3> AND MIO<2>, AND LIO<5> AND MIO<3>, RESPECTIVELY

FIG. 13A

SIMPLE 1 CROSS POINT SENSE AMPLIFIER ALTERNATELY ARRANGED ARRAY

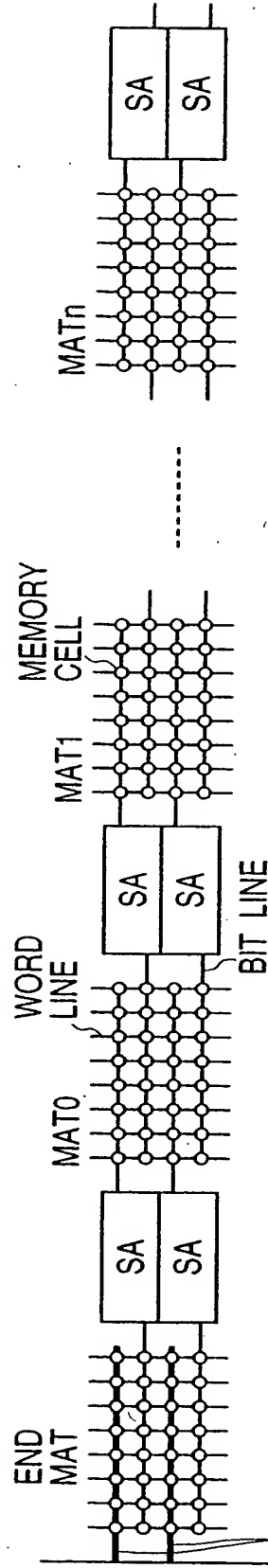


FIG. 13B

PROPOSED FOLDED TYPE ARRAY

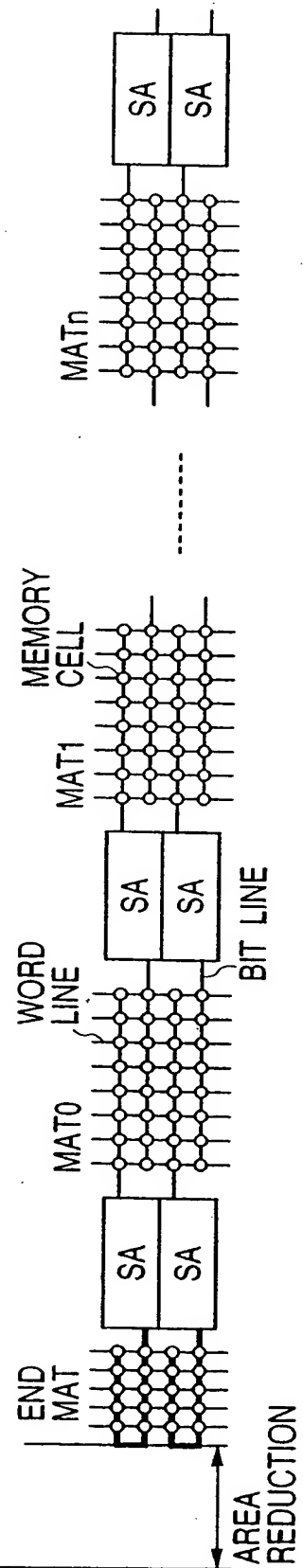


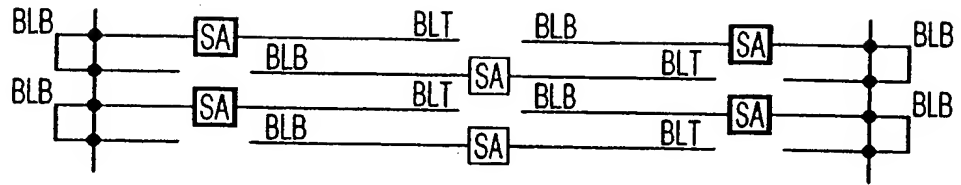
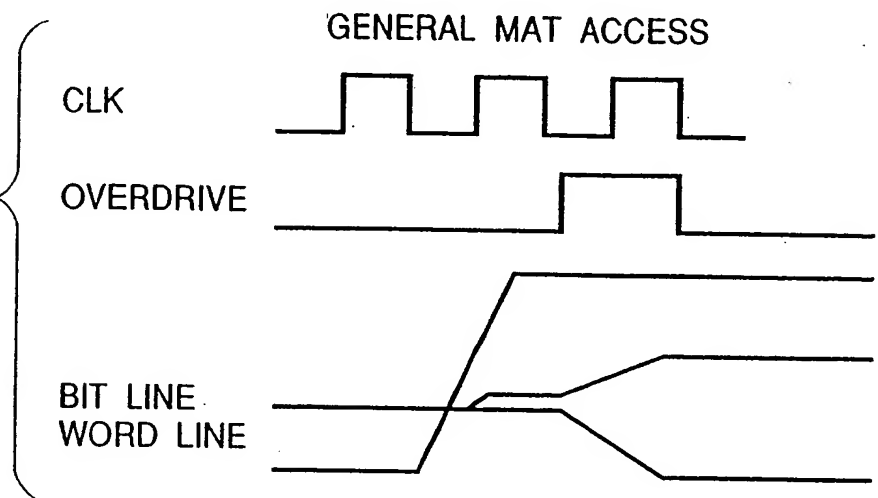
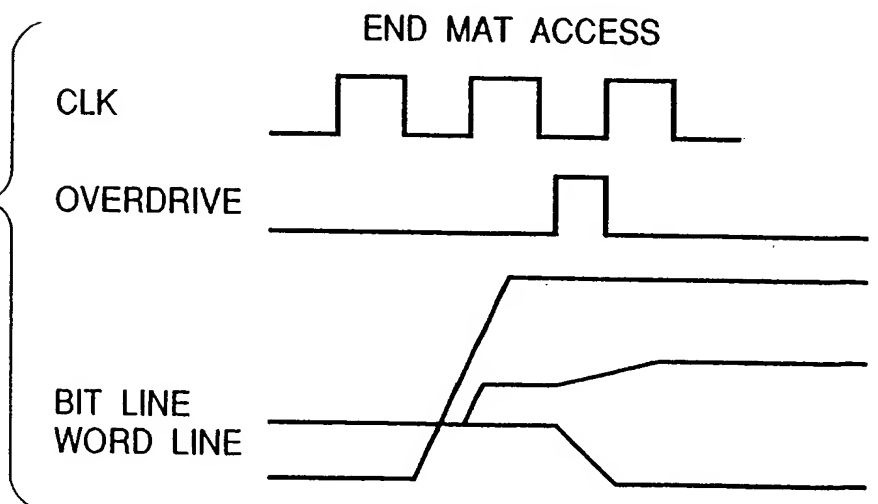
FIG. 14A**FIG. 14B****FIG. 14C**

FIG. 15

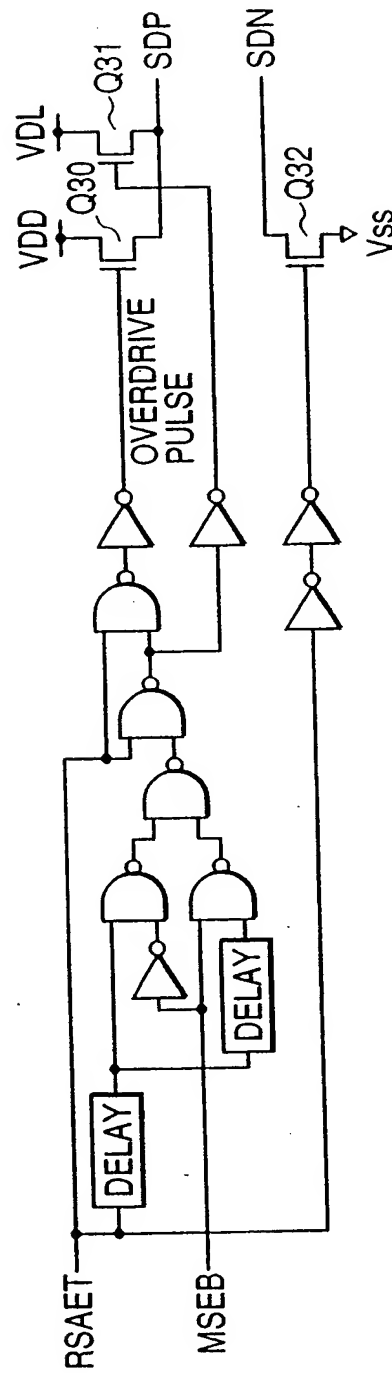


FIG. 16B

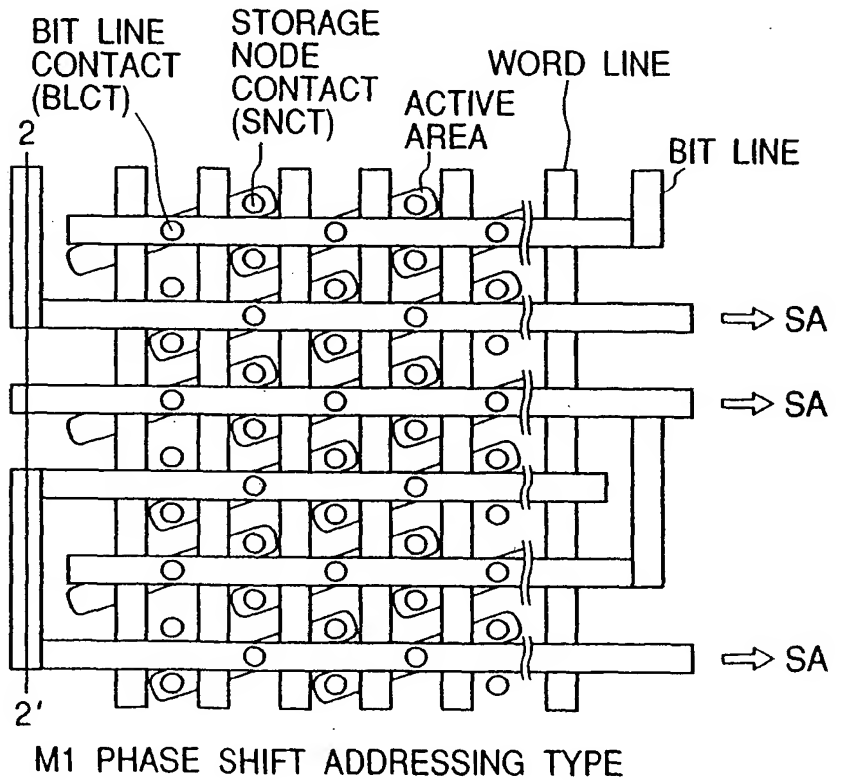


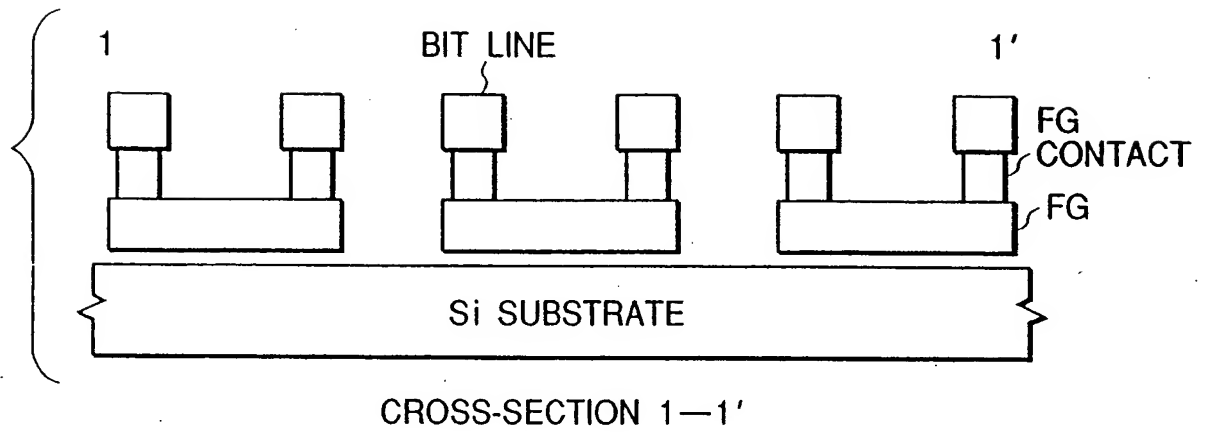
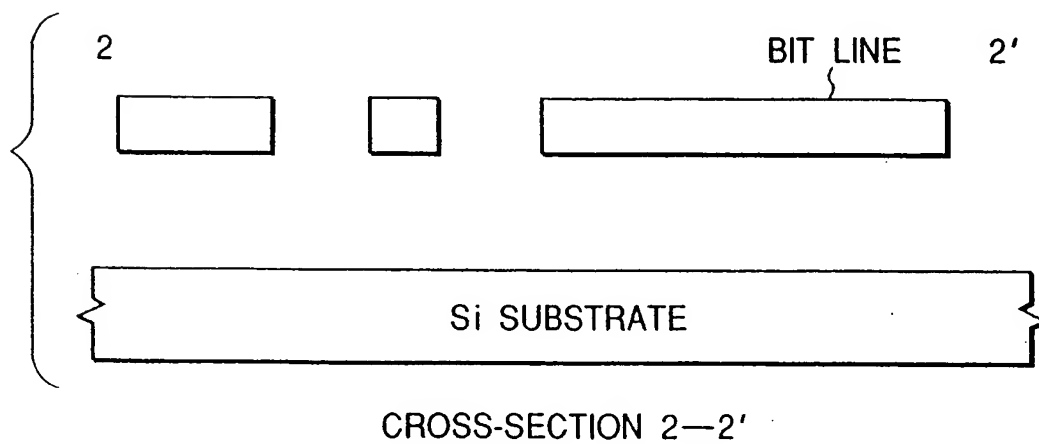
FIG. 17A*FIG. 17B*

FIG. 18

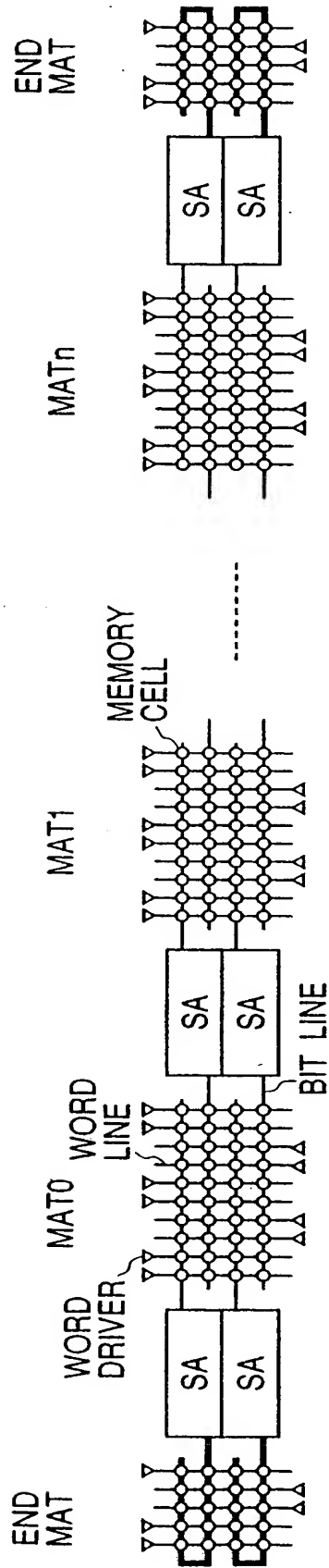


FIG. 19

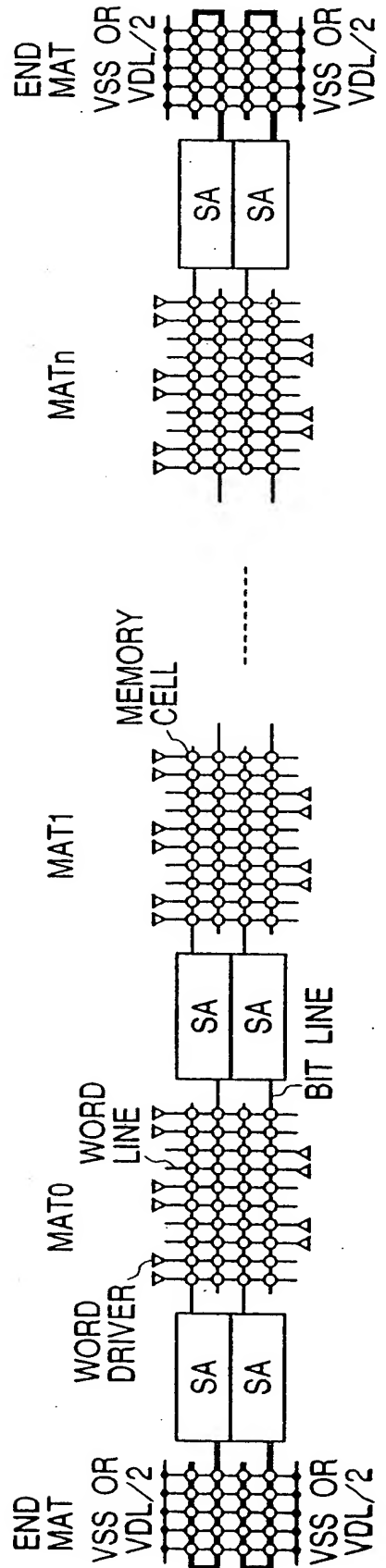


FIG. 20

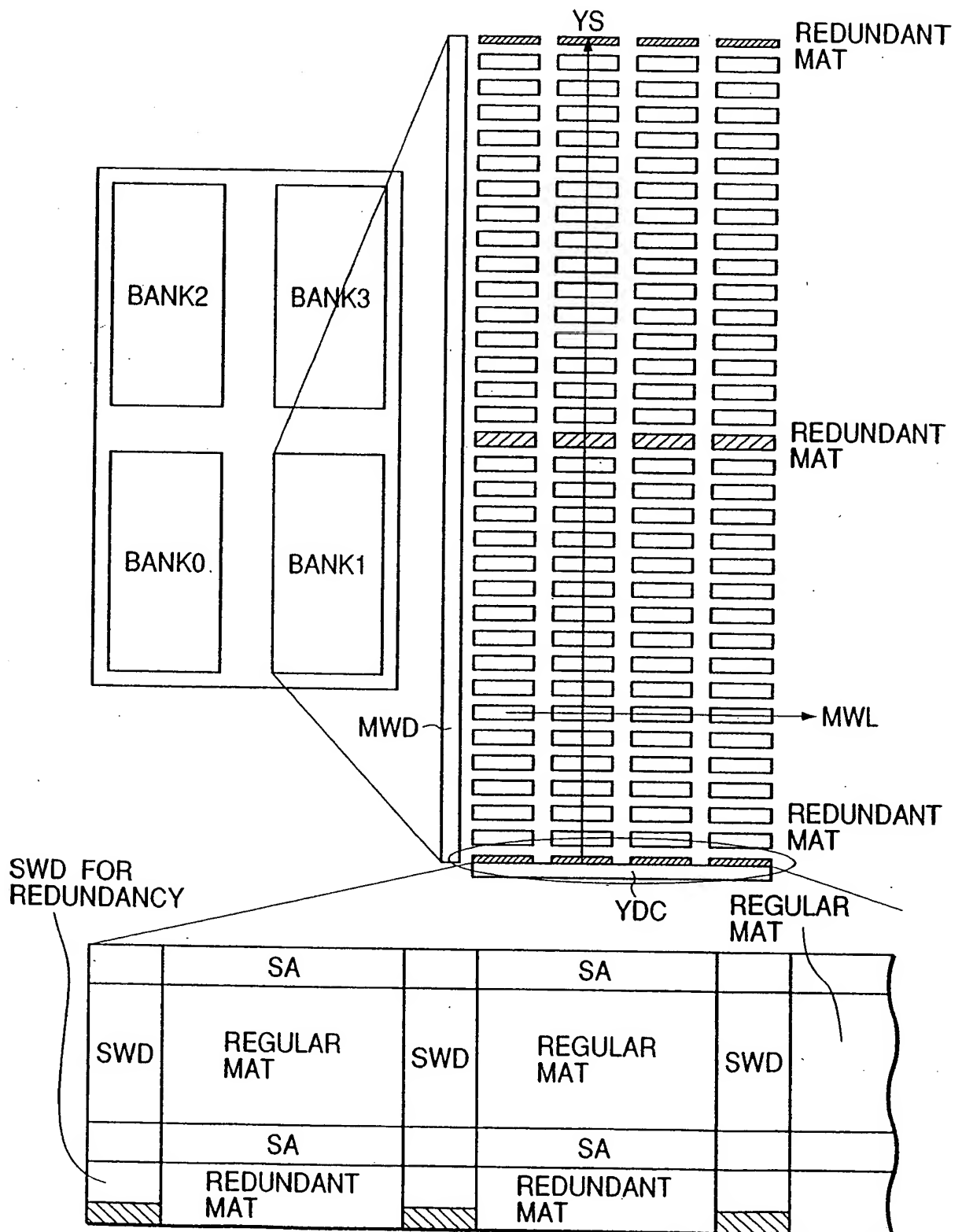


FIG. 22

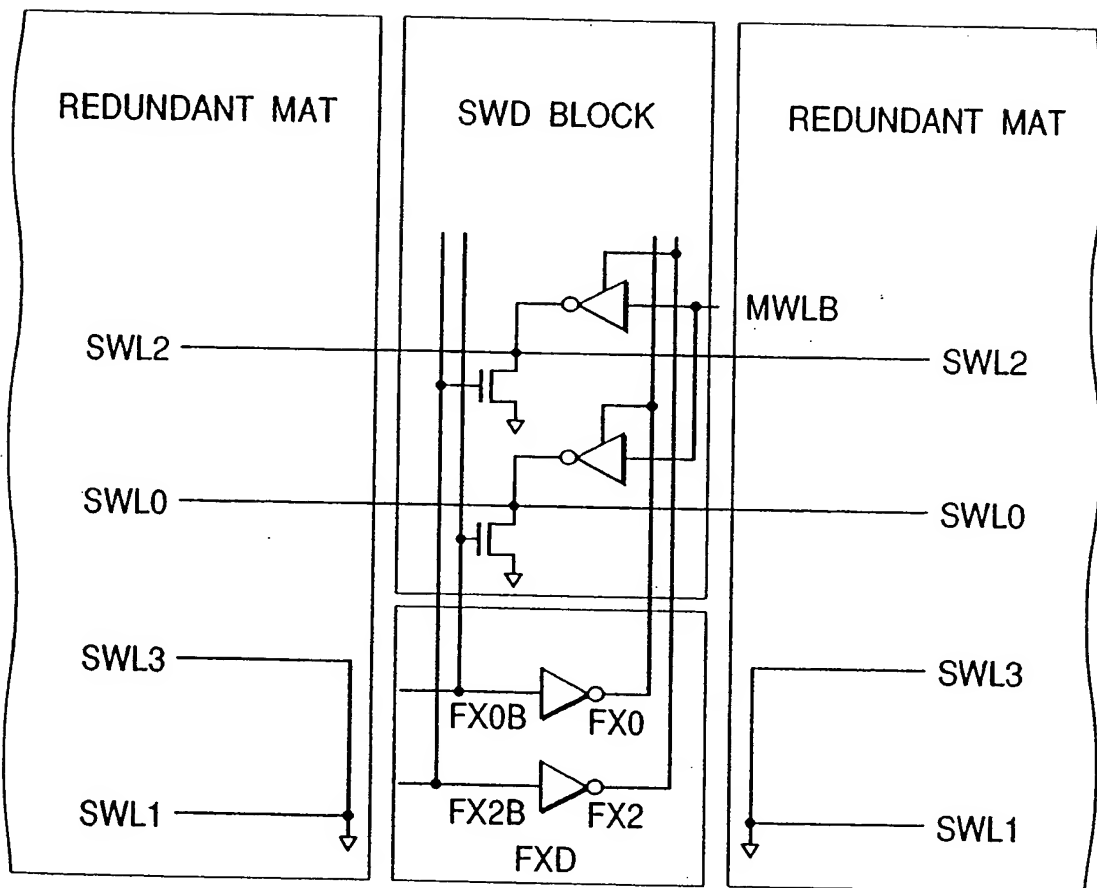


FIG. 23

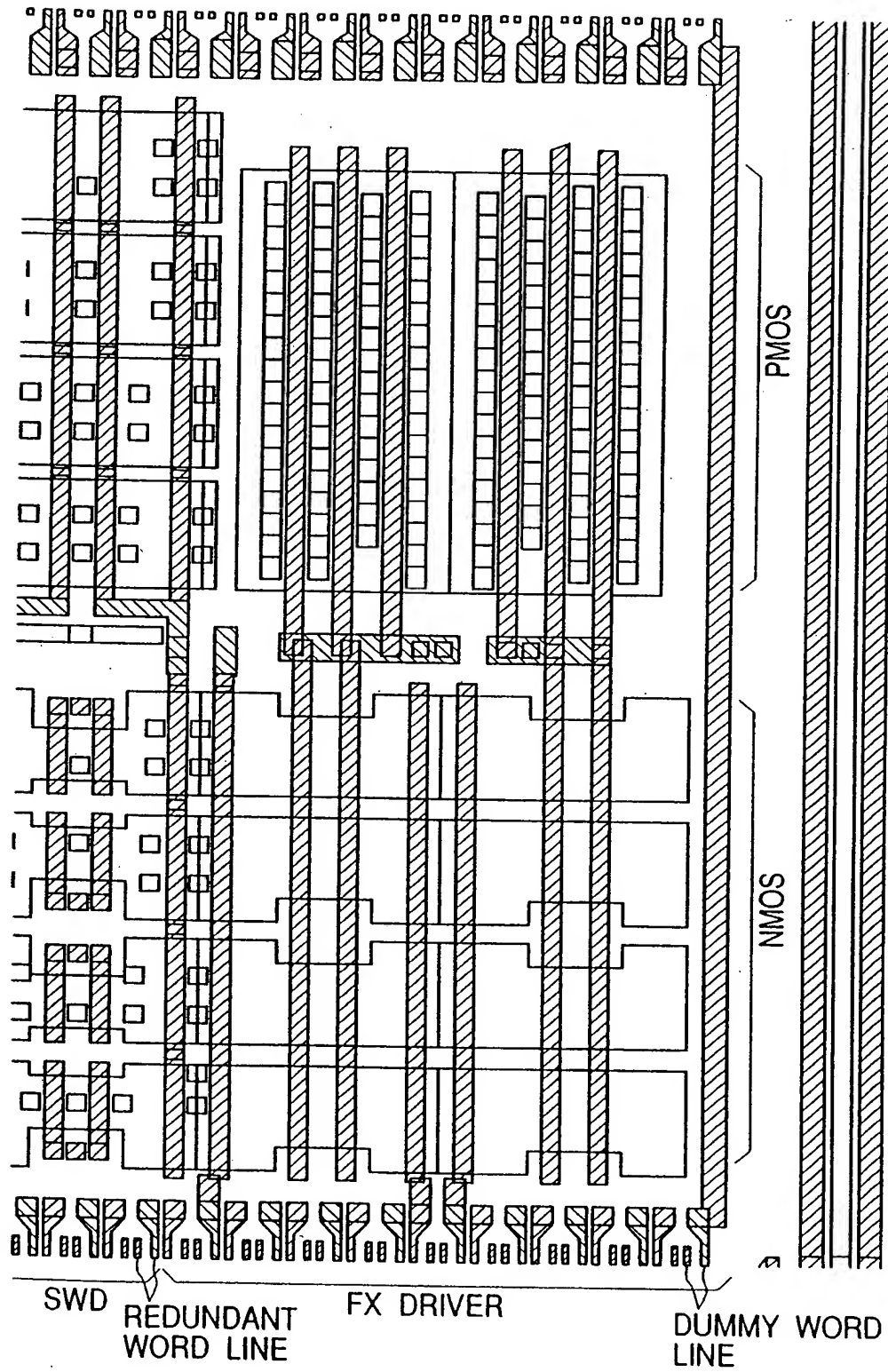


FIG. 24

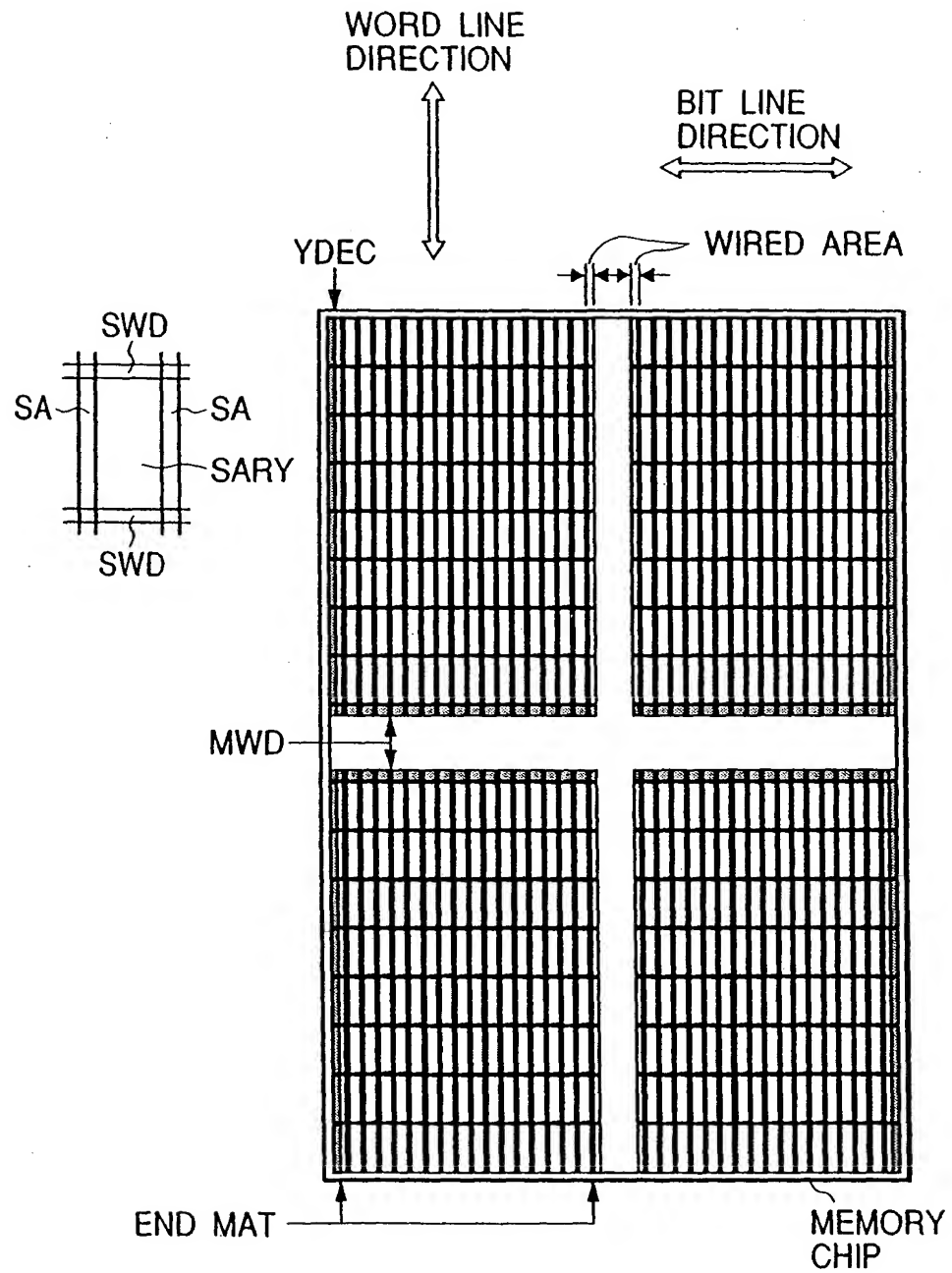


FIG. 25

